TCAD Simulation of Digital Logic Gates in Independent Double Gate Transistors – A Comparative Study between Conventional and Junctionless FETs

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***Abstract*—In this work, conventional independent double gate structure and Junctionless independent double gate structure-based inverters and NAND gates are studied and compared using TCAD simulation. The Junctionless device-based circuits show a larger delay with smaller dynamic power whereas the conventional device-based circuits show smaller delay with larger dynamic power which is a simple power-delay trade-off.**

***Index Terms*—Junctionless FET, FinFET, NAND, inverter, TCAD.**

I. Introduction

Problems faced in the CMOS scaling forces us to move towards multi-gate structures with ultra-thin silicon film. They may be the unique option likely to overcome short channel effects and to provide the possibility of still downscaling CMOS devices into nanometre regime. Multi-gate structures can be of two types, namely simultaneously driven DG (SDDG) and independently driven DG (IDDG) [1]. As the name suggest, simultaneously driven double gate FinFET is a double gated device where the gates are simultaneously driven. In independently driven double gate structure the two gates can be biased separately. Another novel device has been introduced by Collinge et.al. [2], called Junctionless devices which are basically accumulation-mode transistors are gaining importance today. As the name suggests there is no PN junction involved in the Junctionless devices. Desired threshold voltage is achieved by tuning the gate electrode work function. The junction-less transistors have better DIBL characteristics than the conventional double gate FETs.

In independent double gate devices, the threshold voltage of one gate can be modified by giving a bias to another gate. This feature of threshold modification makes the independent gate structures more interesting and many interesting circuit applications have been developed both in digital and analog domains [3], [4]. They deal with the independent structures in conventional double gate devices. In this paper, we compare the performance of basic digital logic gates, inverter, NAND, based on independent double gate Junctionless device with the independent double gate conventional device. Next section deals with the simulator and simulation methodology. In section 3 results are discussed and finally section 4 provides conclusions of the work.

II. Simulator and Simulation Methodology

A. TCAD Simulator

Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. The simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation.
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations.
- Inspect and Tecplot: To view the results.

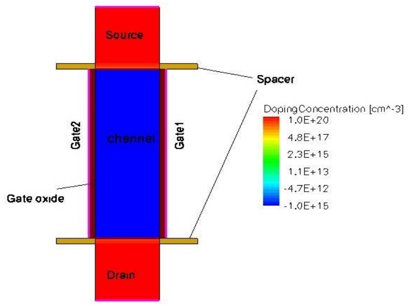

Fig. 1. 2D Structure of conventional N channel independent double gate.

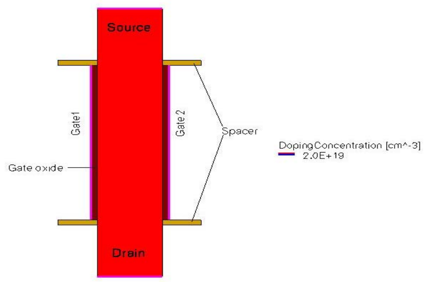

Fig. 2. 2D Structure of Junctionless N channel independent double gate.

The physics section of SDEVICE includes the appropriate models for quantization of inversion layer charge, doping dependency of mobility, effect of high and

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normal electric fields on mobility, and velocity saturation.

Figures 1 and 2 show the 2d structure of conventional N channel independent double gate structure and Junctionless N channel independent double gate structure respectively. The device dimensions and the required work functions for N and P channel devices are tabulated in Table I.

TABLE I: DIMENSIONS OF DEVICE

Parameters	Conventional FinFET	Junction less FET
Gate length (Lg)	30 nm	30 nm
Fin width (W)	10 nm	10 nm
Gate Oxide thickness (Tox)	1 nm	1 nm
Source Width (SW)	10 nm	10 nm
Source length (SL)	10 nm	10 nm
Channel Doping (N_{ch}) N-type	Boron -1e15	Arsenic-2e19
Channel Doping (N_{ch}) P-type	Arsenic-1e15	Boron-2e19
Source/drain Doping (N_{sd}) N-type	Arsenic-1e20	Arsenic-2e19
Source/drain Doping (N_{sd}) P-type	Boron-1e20	Boron-2e19
Work Function (WF)-NMOS	4.41 eV	5.24 eV
Work Function (WF)-PMOS	4.845 eV	4.043 eV
Gate -source/drain underlap (L_{un})	1 nm	1 nm

B. Simulation Methodology

Figure 3 shows the circuit diagrams of the inverter and NAND gate. As the inverter uses one N and one P device, the independent gate device can be used either as a simultaneous driven structure or as a independent gate structure. When the transistors are connected in parallel (P-devices in NAND gate) the device count can be reduced by replacing the parallel devices with the independent device. The independent gates can be used to reduce the power spent by applying a proper bias to second gate [4]. The input pulse characteristics, like rise time, fall time, logic 1 and 0 values etc are shown in Table II.

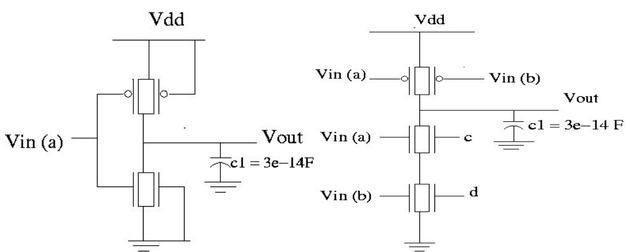

Fig. 3. Circuit diagram of INVERTER and NAND gate.

TABLE II: INPUT PULSE CHARACTERISTICS

Rise time	Fall time	Pulse width	Logic 1	Logic 0
10 ps	10 ps	90 ns	1 V	0 V

C. Caliberation and Id- Vg Characteristics

I_D-V_G characteristics of conventional and Junctionless devices are calibrated against the published results. Figure 4 depicts the I_D-V_G characteristics of conventional and Junctionless devices, for both *N* channel devices and *P* Channel devices. In Fig. 4 gate 2 voltage is kept at zero volts and gate 1 is swept from zero to V_{dd}.

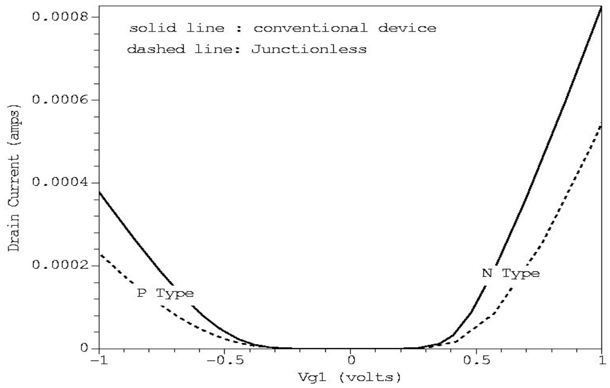

Fig. 4. ID-VG characteristics of conventional and junctionless devices.

III. RESULTS AND DISCUSSION

Figure 5 and 6 show the transient simulation plots of both conventional and Junctionless transistors-based inverter in independently driven mode and in simultaneously driven mode respectively. Table III shows the delays of both conventional and Junctionless devices in simultaneous and independent modes. It can be observed from Table III that delay for conventional device based inverter is less than Junctionless device-based inverter. The reduced current drive of Junctionless device compared to conventional device (refer Fig. 4) can be attributed to this delay degradation in Junctionless device-based inverter. It can also be seen from Table III that independent device based inverter shows more delay compared to simultaneously driven devices. Again the reduction in current driven is the reason for this increased delay in independently driven gate-based inverters. Table III also shows the static and dynamic powers for all the cases discussed above. It can be seen the static power is less in conventional device based inverter is less compared to Junctionless device based inverter. This is expected because the Junctionless devices are bulk conduction devices. The dynamic power comparison of conventional and Junctionless device-based inverters shows the opposite trend and is again expected because of the reduced current drive of Junctionless devices.

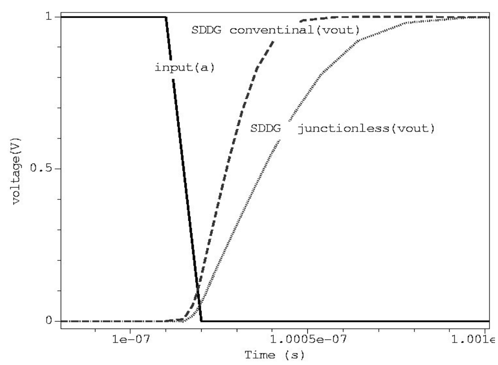

Fig. 5. Transient Simulation plots both conventional and junctionless transistorbased inverter in simulataneously driven mode.

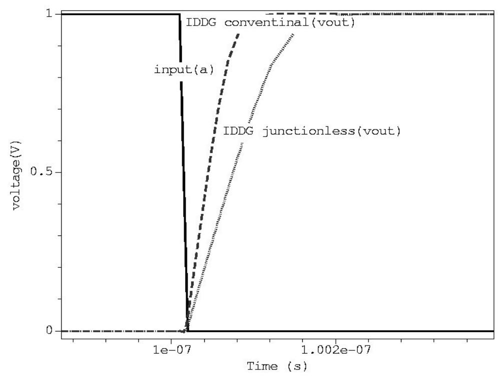

Fig. 6. Transient Simulation plots both conventional and junctionless transistor based inverter in independently driven mode.

Figures 7 and 8 show transient simulation plots of NAND gate both with conventional and Junctionless - based respectively. Table IV gives the delay and power of both conventional and Junctionless device based NAND gates. It can be seen from Table IV that the rise time delay is independent of gate#2 voltage except a small increase whereas the fall time delay decreases with increase in gate#2 bias. This is true for both conventional and Junctionless devices. It is expected that the static power should show a small increase as gate#2 bias increases

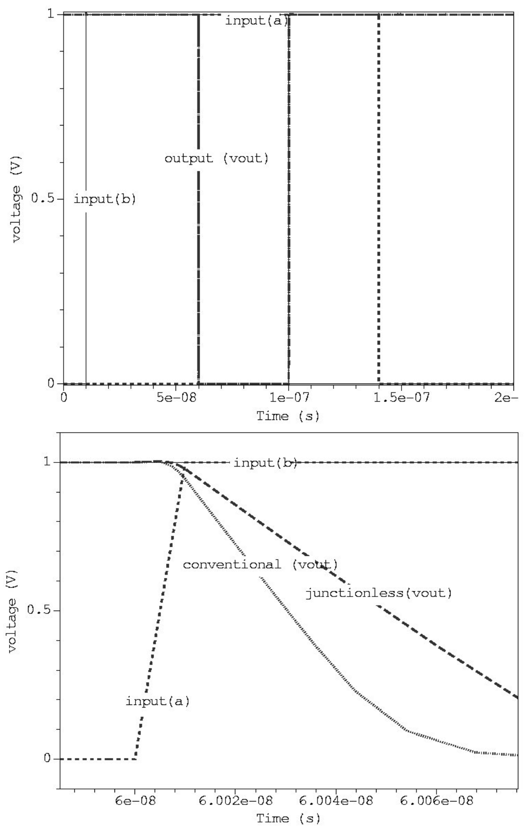

Fig. 7&8. Transient Simulation plots both conventional and Junctionless transistor based NAND gate in independently driven mode & showing transition from logic 1 to logic 0.

TABLE III: DELAY AND POWER OF CONVENTIONAL AND JUNCTIONLESS BASED INVERTER

Device	Delay (ps)		Power			
	SDDG	IDDG	Static Power (nw)		Dynamic power (μw)	
			SDDG	IDDG	SDDG	IDDG
conventional	20	57	12.7	12.69	1215	561.7
Junctionless	43	120	16.3	16.18	700.6	275.7

TABLE IV: DELAY AND POWER OF CONVENTIONAL AND JUNCTIONLESS BASED NAND GATE

Different gate2 bias conditions	Device	Delay (ps)	Power	
			Static Power (nw)	Dynamic power (μw)
c = - 0.1 V d = - 0.1 V	conventional	57	19.59	489.6
	Junctionless	117	33.6	246.5
c = 0 V d = 0 V	conventional	59	20.37	490.97
	Junctionless	121	35.4	230.9
c = 0.1 V d = 0.1 V	conventional	59	27.59	484.78
	Junctionless	118	33.8	219.5

IV. CONCLUSION

Using conventional independent double gate structure and Junctionless independent double gate structure an inverter and NAND gate were realized in TCAD simulation. Even though the Junctionless device-based circuits show a larger delay the dynamic power consumption is smaller which means that it is a simple power-delay trade-off. So the Junctionless devices can be the potential alternative for the conventional inversion mode MOS device.

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REFERENCES

[1] M. Shrivastava, M. S. Baghini, A. B. Sachid, D. K. Sharma, and V. R. Rao, "A Novel and Robust Approach for Common Mode Feedback using IDDG FinFET," *IEEE Transactions on Electron Devices,* vol. 55, no. 11, pp 3274-3282, November 2008.

[2] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," *IEEE Journal of solid state circuits,* vol. 54, pp. 97–103, 2010.

[3] L. Mathew, Y. Du, A. V.-Y. Thean, M. Sadd, A. Vandooren, C. Prher, T. Steehehens, R. Mm. R. Rar, M. Zavala, D. Sing, S. Kafwl, J. Hughes, R. Shimer, S. Jaflepalfi, F. Wmmen, W. Zhangz, and Y. Nguyen, “CMOS Vertical Multiple Independent Gate Field Effect Transistor (MIGFET),” *IEEE International SO1 Conference,* April 2004.

[4] A. Muttreja, N. Agarwal, and N. K. Jha, "CMOS logic design with independent gate finfets," *25th international conference on computer design,* pp 560-567, ICCD 2007.

[5] Synopsys Sentaurus TCAD user manual.