# A New Circuit Model of Small-Signal Sziklai Pair Amplifier

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***Abstract*—A new circuit model of RC coupled small-signal Sziklai pair amplifier is proposed and qualitatively analyzed for the first time. The circuit of proposed amplifier uses a Sziklai pair with NPN driver and crops high voltage gain (237.916), moderate bandwidth (15.10KHz), fairly high current gain (712.075) and considerably low THD (0.73%) at 1mV, 1KHz input AC signal. This circuit can be tuned in specific audible frequency range, extending approximately from 1Hz to 20KHz. Tuning performance makes this amplifier circuit suitable to use in Radio and TV receiver stages. The qualitative and tuning performance of the proposed amplifier offers it a flexible application range as high voltage gain, high power gain and tuned amplifier. Tuning performance, variation of voltage gain with frequency and different biasing resistances, input and output noises at operating frequency, temperature dependency of performance parameters and total harmonic distortion of the amplifier are perused for providing wide spectrum to the qualitative studies. The proposed Sziklai pair configuration with NPN driver transistor can be attempted to fabricate a single pack transistor IC version of Sziklai pair. Proposed circuit is also free from poor response problem of small-signal Darlington pair amplifiers at higher frequencies and narrow-band response region for PNP driven small-signal Sziklai pair amplifier.**

***Index Terms*—Small signal amplifiers, sziklai amplifiers, complementary darlington pair amplifiers.**

## I. Introduction

Amplification of signals through Darlington pair and Sziklai pair is an important phenomenon of electronics [1]-[8]. A Darlington pair holds two identical BJTs in CC-CE connection and its application range virtually extends from small-signal amplifiers to power amplifier circuits [1], [2], [5], and [9]. However, Sziklai pair unit uses two BJTs of opposite polarities (one NPN and other PNP transistor) in CE-CE connection and therefore, sometimes known as Complementary Darlington pair [3], [4], [7], [8]. Polarity of this compound configuration, which is a popular unit to use in power amplifiers rather than small-signal amplifiers, is always determined by the driver transistor [3], [7], [8]. Therefore, a Sziklai pair having PNP driver and NPN output transistor behaves like a PNP transistor and vice versa [3], [7], [8].

Principally, both the paired units enjoy high input resistances, low output resistances and voltage gains approximately equal to unity [1], [4], [7].

However, due to small amount of in-built negative feedback, the current gain factor of Sziklai pair ($\beta_{Szk}=\beta_{Q1}\beta_{Q2}+\beta_{Q1}$) is slightly less than Darlington pair ($\beta_{Dar}=\beta_{Q1}\beta_{Q2}+\beta_{Q1}+\beta_{Q2}$) topology but at higher values of $\beta$ (normally for $\beta$>100) both are approximated to $\beta\approx\beta_{Q1}\beta_{Q2}$ [1], [4], [7]. These paired units of vital importance are often compared due to almost identical ranges of current gain, input resistance, output resistance and voltage gain but possess several disparities in appearance and qualitative features [1], [4], [7], [8]. For example, Sziklai pairs hold better linearity than Darlington pairs when used in linear circuits [4], [7]. Similarly, the base turn-on voltage of Sziklai pair is only half of the Darlington's turn-on voltage [4], [7], [8].

In electronics industry, Sziklai pairs are normally used in push–pull output stage of power amplifiers [1] and [4]. However, researches towards the development of small-signal amplifiers using Sziklai pair and to propose a scheme for an integrated version of Sziklai pair as a single transistor are almost untouched [7], [8]. Contrary to this, authors have recently developed a small-signal Sziklai pair amplifier [7] with PNP driver. This circuit [7] produces high voltage gain, removes the problem of poor response of small-signal Darlington pair amplifier at higher frequency but shows a response in narrow-band frequency region [7], [8].

The present investigation is focused around a Sziklai pair which uses one NPN and other PNP transistor in its composite unit [4], [7]. This Sziklai pair with NPN driver and appropriate biasing components is explored as new circuit model of a small-signal amplifier suitable for radio and TV receiver stages.

## II. Experimental Circuits

Present work comprises a qualitative comparison between two different circuits of small-signal Sziklai pair amplifiers [7], [8]. The first circuit having PNP driver transistor (Fig. 1) is named here as Reference amplifier [7], [8] whereas the proposed amplifier, having NPN driver transistor, is depicted in Fig. 2.

Reference amplifier is qualitatively observed with an additional biasing resistance $R_A$ [7], [8], [10], [11], connected between collector of Q1 and ground. However, observations for proposed amplifier are taken without additional biasing resistance $R_A$ [7], [8], [10], and [11] but the effect of $R_A$ (175KΩ) on voltage gain, current gain, bandwidth and THD is discussed to strengthen qualitative studies. This resistance $R_A$ in the proposed amplifier is optional in nature and can be introduced between collector of *Q*1 and $V_{CC}$ (depicted by

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dotted lines). Similarly, tuning performance of the proposed circuit is observed by introducing a variable capacitor $C_L$ across load resistance $R_L$ (shown by dotted lines).

Amplifier circuits under discussion use potential divider biasing methodology [7], [9]-[11], [13] and are configured with suitably selected passive biasing components to provide proper DC biasing. Component details of the respective amplifier circuits are summarized in Table I.

TABLE I: CONFIGURATION DETAILS AND BIASING PARAMETERS

| Components | Circuit of Fig. 1 | Circuit of Fig. 2 |
|---|---|---|
| Q1 | Q2N2907A | Q2N2222 |
| Q2 | Q2N2222 | Q2N2907A |
| $R_S$ | 500Ω | 500Ω |
| $R_1$ | 33KΩ | 100KΩ |
| $R_2$ | 100KΩ | 47KΩ |
| $R_{CE}$ | 10KΩ | 9KΩ |
| $R_E$ | 2KΩ | 5KΩ |
| $R_A$ | 500Ω | 175KΩ (Optional) |
| $R_L$ | 10KΩ | 10KΩ |
| $C_1$, $C_2$ | 1 µF | 10 µF |
| $C_L$ (Variable) | - | 1pF-1nF |
| $C_E$ | 0.1 µF | 100 µF |
| Biasing Supply | +18V DC | +25V DC |
| AC Signal range | 10-30mV (1KHz) | 0.1-12mV (1KHz) |

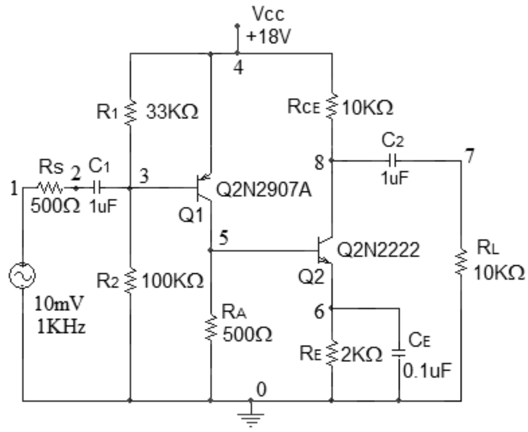


Fig. 1. Reference amplifier (PNP Sziklai pair).

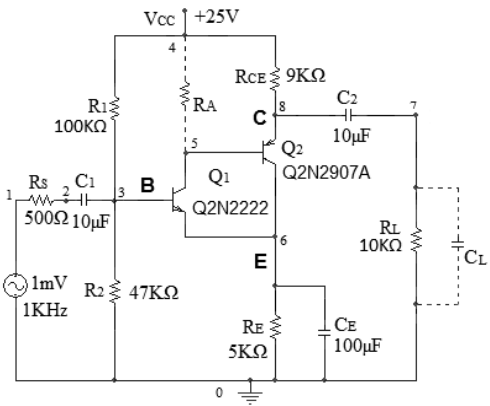


Fig. 2. Proposed amplifier (NPN Sziklai pair).

PSpice simulation (Student version 9.2) is performed to carry out present investigations [7]-[12]. Observations are procured by feeding the amplifier circuits with 1V AC input signal source, from which, a small-distortion-less AC signal of 10mV for reference amplifier (Fig. 1) and 1mV for proposed amplifier (Fig. 2) at 1KHz frequency is drawn as input for amplification purpose. The amplifier of Fig. 1 is found to provide undistorted output for 10-30mV AC input signal at 1KHz frequency whereas proposed amplifier of Fig. 2 produces distortion-less results for 0.1-12mV AC input at similar frequency.

## III. OBSERVATIONS AND DISCUSSIONS

### A. Qualitative Performance

Fig. 3 shows the variation of voltage gains of respective amplifiers with frequency. Clearly, the proposed circuit holds an improved response than reference amplifier. The proposed amplifier of Fig. 2 (without $R_A$) produces 237.916 maximum voltage gain $A_{VG}$ (with peak output voltage $V_{OP}$=242.425mV), 712.075 maximum current gain $A_{IG}$ (with peak output current $I_{OP}$=24.245 µA) and 15.10 KHz bandwidth (with lower-cut-off frequency $f_L$=81.517 Hz and upper-cut-off frequency $f_H$=15.182 KHz). However, the reference amplifier [7], [8] of Fig. 1 produces 102.309 $A_{VG}$ (with peak output voltage $V_{OP}$ =1.106V), 7.345 $A_{IG}$ (with peak output current $I_{OP}$=110.6 µA) and 4.80 KHz bandwidth (with $f_L$=210.108 Hz and $f_H$=5.0153 KHz). Respective values of voltage and current gains logically set the power gain of the proposed and reference amplifiers considerably larger than unity [7], [11].

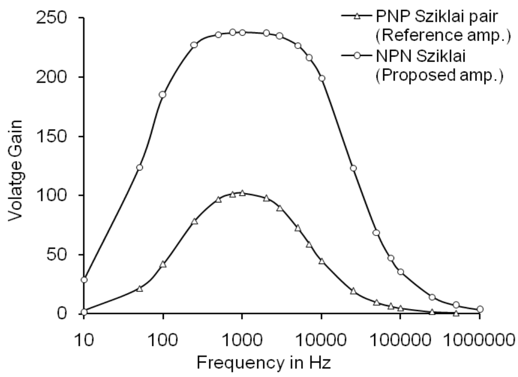


Fig. 3. Variation of Voltage gain with frequency.

Total Harmonic Distortion (THD) for the mentioned circuits are also estimated by following established rule [7]-[8], [11].

$$\%n^{th}\ harmonic\ distortion = \%D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

Respective computations suggest that the reference amplifiers holds 1.72% THD for 8 significant terms [7], [8] whereas the proposed amplifier possesses 0.73% THD for 10 significant terms. Thus, the proposed amplifier (without $R_A$) presents enhanced voltage gain, wider bandwidth, sufficiently larger current gain and considerably reduced THD than reference amplifier. The proposed circuit is also free from the poor response problem of small-signal Darlington pair amplifier at higher frequencies and scenario of narrow-band response for small-signal Sziklai pair amplifier with PNP driver [2], [5], [7], [8], [10], [11].

In succession, when an additional biasing resistance ($R_A$=175KΩ) is included in proposed circuit of Fig. 2, the amplifier enjoys enhancement in $A_{VG}$ to 399.268 (with $V_{OP}$= 398.176mV), $A_{IG}$ to 744.407 (with $I_{OP}$=39.792 µA) and bandwidth to 78.810 KHz (with $f_L$=142.410Hz and

$f_H$=78.810 KHz) but with simultaneously enlarged THD (1.17% for 10 significant harmonic terms).

It is noteworthy that the presence of additional biasing resistance $R_A$ is essential for reference amplifier to retain its explored qualitative features. By virtue of its position, $R_A$ restricts the usage of Sziklai pair of reference amplifier as a single transistor integrated version. However, the use of $R_A$ for the proposed amplifier is optional. Thus, the configuration of Sziklai pair having NPN driver transistor Q2N2222 and PNP follower transistor Q2N2907A, in proposed amplifier without $R_A$ (enclosed between C-B-E in Fig. 2), can be attempted to fabricate a single transistor integrated version of Sziklai pair.

In addition, when few of the biasing parameters of proposed amplifier of Fig. 2 (without $R_A$) are changed to $R_S$=100Ω, $R_2$=33KΩ, $R_{CE}$=6KΩ, $R_E$=2KΩ, $C_1$=$C_2$=1 $\mu F$; $A_{VG}$ of the circuit rises to 334.921 (with $V_{OP}$ =337.861mV), $A_{IG}$ to 746.533 (with $I_{OP}$=33.796µA) bandwidth to 16.141KHz (with $f_L$=149.733Hz and $f_H$=16.291KHz) and THD to 1.21%. Successively, when similar configuration is tested with an added resistance $R_A$ of 47KΩ (between node 5 and 4), the $A_{VG}$ of the circuit rises further to 476.092 (with $V_{OP}$=467.252mV), bandwidth to 278.135KHz ($f_L$=239.841Hz and $f_H$=278.375KHz), THD to 2.06% but $A_{IG}$ of the circuit reduces to 388.442 (with $I_{OP}$=46.773µA).

TABLE II: VARIATION OF AVG,AIG AND BANDWIDTH WITH TEMPERATURE

| Temp (℃) | Reference Amplifier (PNP Sziklai) | | | Proposed Amplifier (NPN Szikali) | | |
|---|---|---|---|---|---|---|
| | $A_{VG}$ | $A_{IG}$ | Bandwidth (KHz) | $A_{VG}$ | $A_{IG}$ | Bandwidth (KHz) |
| -30 | 83.43 | 5.742 | 4.73 | 288.85 | 792.01 | 20.71 |
| -20 | 86.93 | 6.029 | 4.75 | 278.29 | 779.66 | 19.84 |
| -10 | 90.36 | 6.314 | 4.76 | 268.53 | 766.17 | 18.64 |
| 0 | 93.70 | 6.596 | 4.78 | 259.46 | 751.99 | 17.58 |
| 10 | 96.96 | 6.876 | 4.79 | 251.01 | 737.36 | 16.61 |
| 27 | 102.31 | 7.345 | 4.80 | 237.92 | 712.07 | 15.10 |
| 50 | 109.12 | 7.962 | 4.81 | 222.43 | 678.29 | 13.41 |
| 80 | 117.22 | 8.734 | 4.86 | 205.19 | 636.42 | 11.57 |

Therefore, the inclusion of additional biasing resistance $R_A$ in the proposed circuit of NPN Sziklai pair amplifier at any biasing combination considerably improves the status of voltage gain and bandwidth but on the cost of simultaneously enhanced THD.

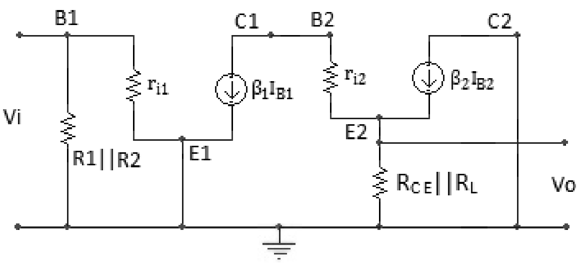


Fig. 4. AC equivalent circuit of proposed amplifier.

Small-signal AC equivalent circuit of proposed amplifier is drawn in Fig. 4. AC analysis of this amplifier (without $R_A$) shows that its equivalent output impedance $Z_O \approx R_O.r_{i1}/(\beta_1\beta_2R_O+r_{i1})$ is lower (≈17.80Ω) than the equivalent input impedance $Z_I \approx R_1||R_2||r_{i1}$ (≈ 29.05KΩ), with a phase reversal in output voltage waveform. In addition, AC voltage gain of the proposed amplifier is estimated to $A_V \approx -R_O.(\beta_1\beta_2+\beta_1)/r_{i1}$ and therefore figured out to be-266.214 [1]. Here the computed $R_O$=$R_{CE}||R_L$=4.73KΩ, $\beta_1\beta_2+\beta_1$=17898 and $r_{i1}=(\beta x26mV)/I_E$=318.4KΩ, for the circuit of Fig. 2. Negative sign in the expression shows phase reversal of the output voltage which is because the composite unit of Sziklai pair holds an equivalent CE configuration [1].

Variations of $A_{VG}$, $A_{IG}$ and bandwidth with respect to temperature (in the range of -30°C to 80°C) are also measured and listed in Table II. For reference amplifier, the bandwidth remains almost unchanged but both varieties of gains increases with rising temperature [7], [8]. This verifies the usual behavior of transistor parameter $h_{FE}$ with temperature [14]. However for proposed amplifier, both varieties of gain and bandwidth decrease with temperature elevation. This contrast behavior of Fig. 2 amplifier at rising temperature is due to the absence of additional biasing resistance $R_A$ and the differently chosen values of $R_1$ and $R_2$ compared to the reference amplifier.

The DC current gain factor $\beta_Z$ and forward current transfer ratio $\alpha_Z$ for the composite units of Fig. 1 and Fig. 2 amplifiers at different temperatures are also calculated using following expressions [4], [7]. Respective results are summarized in Table III along with DC current gain factor $\beta_Q$ of various transistors in Fig. 1 and Fig. 2.

$$\beta_z = \beta_{Q1}\beta_{Q2} + \beta_{Q1}$$

$$\alpha_Z = \frac{\beta_Z}{(1+\beta_Z)}$$

DC current gain factor $\beta_{Q1}$ for both the circuits and $\beta_{Q2}$ for proposed circuit increases with temperature whereas $\beta_{Q2}$ for reference amplifier decreases. The presence of additional biasing resistance $R_A$ in reference amplifier increases the base current to transistor $Q2$ which further elevates with temperature and therefore reduces $\beta_{Q2}$.

TABLE III: VARIATION OF A AND B WITH TEMPERATURE

| Temp (℃) | Reference Amplifier | | | | Proposed Amplifier | | | |
|---|---|---|---|---|---|---|---|---|
| | $\beta_{Q1}$ | $\beta_{Q2}$ | $\beta_Z$ | $\alpha_Z$ | $\beta_{Q1}$ | $\beta_{Q2}$ | $\beta_Z$ | $\alpha_Z$ |
| -30 | 172 | 0.211 | 208 | 0.995 | 60.1 | 166 | 10037 | 0.999 |
| -20 | 182 | 0.180 | 215 | 0.995 | 63.3 | 176 | 11204 | 0.999 |
| -10 | 192 | 0.154 | 222 | 0.995 | 66.5 | 186 | 12435 | 0.999 |
| 0 | 202 | 0.132 | 229 | 0.995 | 69.7 | 197 | 13801 | 0.999 |
| 10 | 212 | 0.112 | 236 | 0.995 | 72.9 | 208 | 15236 | 0.999 |
| 27 | 229 | 0.083 | 248 | 0.996 | 78.5 | 227 | 17898 | 0.999 |
| 50 | 252 | 0.052 | 265 | 0.996 | 86.1 | 253 | 21869 | 0.999 |
| 80 | 282 | 0.021 | 288 | 0.996 | 96.3 | 289 | 27927 | 0.999 |

In addition, due to typical Sziklai pair configurations, the $\beta$ values corresponding to NPN transistors in reference and proposed amplifiers are considerably less than $\beta$ values for PNP transistors at every temperature. However, $\beta_Z$ for compound unit of both the amplifiers and forward current transfer ratio $\alpha_Z$ of the reference amplifier increases but $\alpha_Z$ of proposed amplifier remains constant at almost ideal value with increasing temperature. The ideal values of $\alpha_Z$ for proposed amplifier in Table III shows its superiority over reference amplifier and verifies the use of proposed circuit configuration as voltage amplifier.

The input and output noises at operating frequency are also observed for both the amplifiers and listed in Table IV. Usually, resistors and semiconductor devices in electronic circuits are responsible to generate noises during amplification process. Table clearly indicates that level of input and output noises is significantly low for respective amplifiers and within the permissible limit but the level of noises for proposed amplifier is found slightly higher than reference amplifier. Respective noises for reference and proposed amplifiers increase with temperature which is an obvious feature due to generation of more carriers and their higher collision rate at elevated temperature.

TABLE IV: VARIATION OF INPUT AND OUTPUT NOISE WITH TEMPERATURE

| Temp. (℃) | Reference Amplifier | | Proposed Amplifier | |
|---|---|---|---|---|
| | $N_{OUT}$ ($10^{-7}$ V/Hz) | $N_{IN}$ ($10^{-9}$ V/Hz) | $N_{OUT}$ ($10^{-7}$ V/Hz) | $N_{IN}$ ($10^{-9}$ V/Hz) |
| -30 | 3.765 | 4.512 | 18.62 | 6.328 |
| -20 | 3.954 | 4.548 | 18.69 | 6.721 |
| -10 | 4.142 | 4.583 | 19.12 | 7.125 |
| 0 | 4.328 | 4.619 | 19.56 | 7.542 |
| 10 | 4.513 | 4.654 | 20.00 | 7.969 |
| 27 | 4.822 | 4.713 | 20.75 | 8.722 |
| 50 | 5.229 | 4.792 | 21.78 | 9.790 |
| 80 | 5.736 | 4.893 | 23.12 | 11.270 |

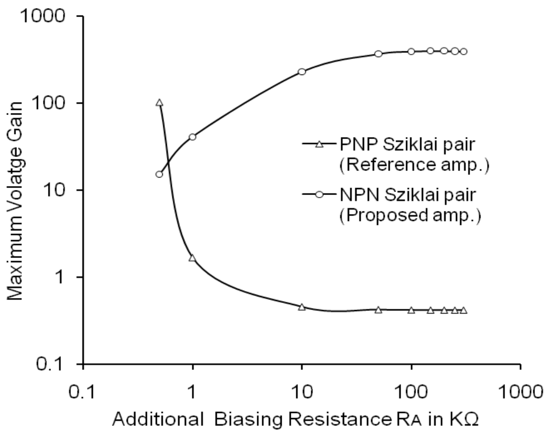


Fig. 5. Variation of maximum voltage gain with added resistance $R_A$.

Variation of maximum voltage gain $A_{VG}$ as a function of added resistance $R_A$ is shown in Fig. 5. The maxim of the voltage gain corresponding to added resistance $R_A$ for PNP Sziklai Pair amplifier of Fig. 1 is observed at $R_A$=*0.5KΩ*, thereafter, it decreases almost exponentially and finally tends towards saturation beyond $R_A$=50KΩ [7], [8]. However, for proposed amplifier of Fig. 2, $A_{VG}$ increases almost non-linearly at elevated values of $R_A$; found its maximum at $R_A$=175KΩ, and thereafter, it tends towards saturation. Sziklai pair configuration and the position of added resistances in respective amplifier circuits are responsible for enhancement in $A_{VG}$ for proposed amplifier and reduction in $A_{VG}$ for reference amplifier. The reason is that as $R_A$ of the reference amplifier is increased, base voltage to NPN transistor *Q*2 (node 5) increases and current through $R_A$ reduces [7], [8]. This increases current through $R_E$ and causes reduction in load current (through $R_L$), which ultimately decreases the maximum voltage gain $A_{VG}$. Similarly, when $R_A$ of the proposed amplifier is increased, base voltage to the PNP transistor *Q*2 (node 5) reduces which in turn increases the collector current of *Q*2 and causes load current and $A_{VG}$ to increase. It is also to be mentioned that the distortion percentage increases with increasing values of $R_A$ for proposed amplifier (it rises from 1.08% at $R_A$=10KΩ to 1.17% at $R_A$=175KΩ).

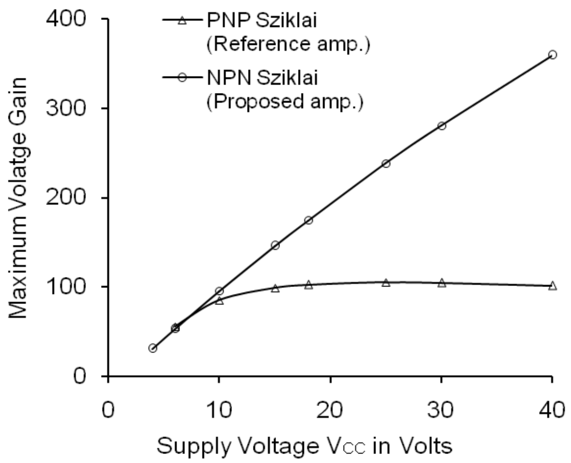


Fig. 6. Variation of maximum voltage gain with DC supply $V_{CC}$.

The effect of DC supply voltage $V_{CC}$ on maximum voltage gain $A_{VG}$ for both the amplifiers is depicted in Fig. 6. Figure clearly indicates that the Sziklai pair unit of reference amplifier switches-ON at 6V and the amplifier produces a fruitful response in 6-40V range of $V_{CC}$. Moreover, the corresponding voltage gain rises gradually with increasing values of $V_{CC}$ and tends towards saturation beyond 18V [7], [8]. However, NPN Sziklai pair unit of proposed amplifier switches-ON at 4V only. The proposed circuit provides distortion-less output in 4-40V range of $V_{CC}$ and the respective voltage gain possesses almost linear rising tendency at increasing values of $V_{CC}$. This happens because on increasing biasing supply $V_{CC}$, the saturation current of respective Sziklai units increase which in turn enhances the current across load resistance $R_L$ and hence the overall voltage gain of amplifiers [7], [8].

Fig. 7 depicts the variation of $A_{VG}$ with $R_E$ for both the amplifiers. The reference amplifier responds fairly for $R_E$<30KΩ [7], [8] whereas proposed amplifier provides distortion-less response for $R_E$<50KΩ. $A_{VG}$ of the reference amplifier increases non-linearly with $R_E$ but it decreases almost exponentially at increasing values of $R_E$ for proposed amplifier. The reason is that as $R_E$ increases for reference amplifier, current through $R_E$ reduces which in turn causes load current (through $R_L$) and therefore $A_{VG}$ to increase. Similarly for proposed amplifier, as $R_E$ increases, current through $R_{CE}$ increases which causes load current (through $R_L$) and therefore $A_{VG}$ to reduce.

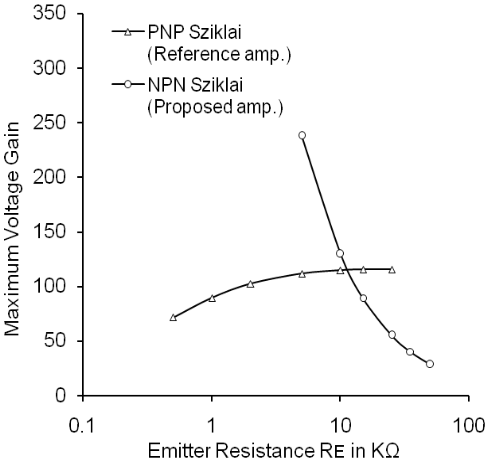


Fig. 7. Variation of maximum voltage gain with emitter resistance.

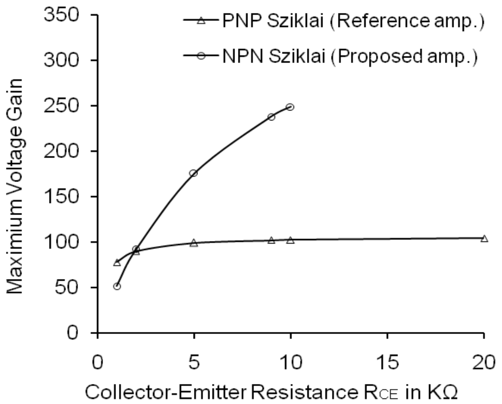


Fig. 8. Variation of maximum voltage gain with collector resistance.

Variations of maximum voltage gain $A_{VG}$ with collector resistance $R_{CE}$ is shown in Fig. 8. It is found that voltage gain has a nonlinear rising tendency for increasing values of $R_{CE}$ for both the amplifiers. For reference amplifier $A_{VG}$ rises up to 5KΩ and beyond this critical limit, it gradually acquires a saturation tendency [7], [8] whereas for proposed amplifier output waveform suffers from distortion beyond 10KΩ of $R_{CE}$. The reason can be explained by the output loop equation [1] for the amplifiers $I_E \approx (V_{CC}-V_{6,8})/(R_{CE}+R_E)$. As $R_{CE}$ increases, $I_E$ reduces which in turn causes load current (through $R_L$) and therefore $A_{VG}$ to increase.

Variations of maximum voltage gain with Load resistance $R_L$ is also estimated but not shown in form of figure. It is observed that voltage gain for both amplifiers rises up linearly up to 50KΩ value of $R_L$ but at higher $R_L$ it gradually acquires a sustained level. This rising and saturation of the voltage gain with $R_L$ is well in accordance of the usual behaviour of small signal amplifiers [5], [7]-[11], [13], [15].

### A. Tuning Performance

Tuning performance of small-signal amplifiers make them suitable to use in designing Radio or TV receiver type systems [16]. Adjusting central frequency of the amplifier's response to match with the frequency of a particular channel, desired signal can be received [16]. Usually in small-signal BJT amplifiers, coupling capacitors $C_1$-$C_2$, emitter by-pass capacitor $C_E$ and load capacitor $C_L$ play crucial role in adjusting bandwidth rather than affecting voltage gain [15].

Tunning performance of the proposed amplifier is established in two steps- first, with $R_E$-$C_E$ network available at the emitter end of $Q1$ (Fig. 2) and second by introducing a tunning capacitor $C_L$ (indicated as doted lines in Fig. 2) across the load $R_L$. Respective observations are listed in Table V and Table VI.

TABLE V: VARIATION OF $A_{VG}$, $A_{IG}$, $F_H$, $F_L$ AND BANDWIDTH WITH TUNING CAPACITOR CE FOR PROPOSED AMPLIFIER

| Tuning capacitor $C_E$ | $f_H$ (KHz) | $f_L$ | Bandwidth (KHz) | $A_{VG}$ | $A_{IG}$ |
|---|---|---|---|---|---|
| 1 µF | 20.92 | 5.77 KHz | 15.14 | 234.39 | 695.84 |
| 10 µF | 15.90 | 775.90 Hz | 15.13 | 237.58 | 710.55 |
| 100 µF | 15.18 | 81.51 Hz | 15.10 | 237.91 | 712.07 |
| 1mF | 15.11 | 8.474 Hz | 15.09 | 237.94 | 712.21 |
| 10mF | 15.11 | 1.582 Hz | 15.10 | 237.94 | 712.16 |

TABLE VI: VARIATION OF $A_{VG}$, $A_{IG}$, $F_H$, $F_L$ AND BANDWIDTH WITH TUNING CAPACITOR CL FOR PROPOSED AMPLIFIER

| Tuning capacitor $C_L$ | $f_H$ KHz | $f_L$ Hz | Bandwidth KHz | $A_{VG}$ | $A_{IG}$ |
|---|---|---|---|---|---|
| 1pF | 15.17 | 81.55 | 15.09 | 237.915 | 712.07 |
| 10pF | 15.14 | 81.53 | 15.05 | 237.911 | 712.06 |
| 100pF | 14.65 | 79.95 | 14.57 | 237.867 | 711.93 |
| 1nF | 11.06 | 81.15 | 10.98 | 237.358 | 710.62 |

Tunning performance of the proposed amplifier with capacitor $C_E$ is obtained for variations between 1 µF and 10mF. Variation in $C_E$ merely creates any change in voltage gain, whereas it changes current gain to some extent and plays a prime role in adjusting the mid-bandwidth. Values of Upper and Lower Cut-off frequencies for different $C_E$ are listed in Table V. It is evident that $f_H$ varies almost in non-significant range whereas $f_L$ considerably shifts towards lower values at increasing $C_E$.

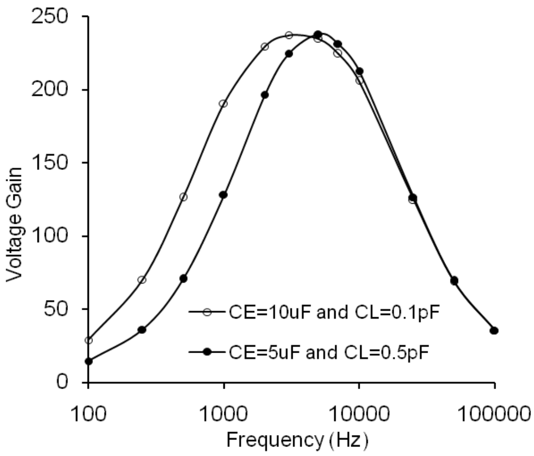


Fig. 9. Tuned frequency response of proposed amplifier at different combination of $C_E$ and $C_L$.

Similarly, inclusion of capacitor $C_L$ across load resistance $R_L$ also plays an important role in adjusting mid-band frequency range for the proposed amplifier. Tunning is obtained for variations of $C_L$ between 1pF and 1nF with a feature that the bandwidth reduces with increase in $C_L$. Voltage gain, current gain and lower-cut-off frequency varies in a very short range for corresponding variations in $C_L$, whereas, the upper-cut-off limit of the bandwidth shifts towards lower values with increasing $C_L$ (Table VI).

Thus, the adjustment of $C_E$ and $C_L$ lead to a tuning which finally ascertain the frequency response of proposed amplifier to peak around a desired frequency. This enables centre frequency of the response to coincide with frequency of a desired communication channel. This tunning idea is depicted in Fig. 9 for two different combinations of $C_E$ and $C_L$. The explored idea of tuning in Fig. 8 leads to a conclusion that NPN driven Sziklai pair configuration in the proposed circuit can be applied to receive signal of a specific channel if proper tunning is established.

## IV. Conclusion

Sziklai pair topology is popularly used to design quasi-complimentary-symmetry push-pull Class-B power amplifiers but in the present manuscript, this topology with NPN Sziklai pair, is first time explored to design a small-signal amplifier. The proposed amplifier circuit is suitable to use in Radio and TV receiver stages due to its tuning performance in the specific range of audible frequency, extending approximately from 1Hz to 20 KHz. The proposed circuit is free from the problem of poor response of conventional Darlington pair amplifiers at higher frequencies and consequently provides an improved bandwidth than small-signal PNP Sziklai pair amplifier (the reference amplifier). Thus, the proposed circuit model can successfully replace conventional circuit model of a small-signal Darlington pair amplifier. The proposed circuit also enjoys higher value of $\beta_Z$ than reference amplifier and holds almost ideal value of $\alpha_Z$. Low order THD of proposed amplifier is another feather in its cap. Moreover, the presence of additional biasing resistance $R_A$ in the proposed circuit of NPN Sziklai pair amplifier considerably improves $A_{VG\text{-}MAX}$ and $A_{IG\text{-}MAX}$ but with the simultaneous enhancement in THD. The proposed amplifier model shows a considerable response for $R_E$, $R_{CE}$, $R_L$ and $V_{CC}$. Additionally, the configuration of Sziklai pair (with NPN driver and PNP follower) in the proposed amplifier circuit without $R_A$ can be significantly attempted to fabricate a single transistor integrated version of NPN Sziklai pair.

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