An Extremely Low Sub-Threshold Swing UTB SOI Tunnel-FET Structure Suitable for Low-Power Applications

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***Abstract*—This paper introduces an Ultra Thin Body Silicon Over Insulator Tunneling Field Effect Transistor structure, which shows excellent device characteristics using a CMOS compatible fabrication process. This fabricated TFET structure shows ≤40 mV Sub-threshold Swing (SS), on-state/ off-state current ratio ≥108 and a scaled down Supply Voltage 0.6 Volt at 32nm gate length. The work also includes a detail design parameters study on the on-state/ off-state current ratio and sub-threshold swing. The result is particularly promising for low-power application of the device.**

***Index Terms*—SOITFET, UTBTFET, band-to-band tunnelling, sub-threshold swing, TCAD.**

I. Introduction

Steep Sub-threshold slope devices are of great interest now a day from energy efficiency point of view. As MOSFET are scaled down, the power supply voltage should also be scaled down in order to reduce the power dissipation of the circuit. In order to achieve this goal while maintaining a suitable on-state and off-state current, the sub-threshold swing of the device must be very low [1]. The sub-threshold swing of the MOSFET is theoretically limited by its 60 mV/decade value. In order to overcome this limiting problem some novel devices have been proposed to achieve a sub-60-mV/dec SS such as impact-ionization MOS devices, nano-electromechanical FET, suspended-gate MOSFETs and tunneling FET [2]. The Tunneling FET (TFET) has been considered as a potential candidate among these novel devices due its carrier transport mechanism of band-to-band tunneling. TFET is considered particularly suitable for low-power application due to its extremely low off-state current and very steep sub-threshold slope [3], [4]. This work presents the process flow for the ultra thin body silicon over insulator TFET structure. Simulation results shows that the ultra thin body silicon over insulator TFET structure exhibits a marked improvement in Ion and sub-threshold swing.

II. Device Structure

Fig. 1 illustrates the UTB SOI TFET structure which is introduced in this paper. The structure has pick source, channel and drain doping 1×10^{20} (Boron), 1×10^{14} (Boron), 5×10^{18} (Phosphorus) respectively. The HfO2 and Aluminum are used as gate insulator and gate metal respectively. Both the gate metal and gate insulator thickness are chosen to be 1nm. A 2nm thick SiO_2 layer has been introduced exactly below the gate region and the channel thickness is chosen as 4nm. The gate has an overlap of 3nm with source and drain regions. A Silicon-Germanium layer is used in the source with Germanium mole fraction and concentration as 0.75 and 1×10^{20} respectively.

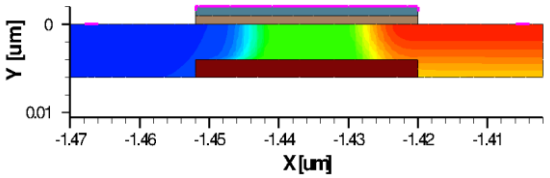

Fig. 1. UTB-SOI TFET structure.

III. Process Flow

All the simulations were carried out in 2D using Sentaurus TCAD. By using the Sentaurus Process, the UTB SOI TFET structure shown in Fig. 1 is achieved.

A. Substrate Oxidation and Etching

First a Silicon substrate is taken with 4nm thickness and 68nm width. A 2nm thick SiO2 is grown on the surface by thermal oxidation.

Then the oxide is etched out from both the side which gives 32nm oxide length as shown in Fig. 3. This oxide will serve as bulk oxide of the device. Next a 6nm thick Silicon is deposited on the structure and additional Silicon is etched out from the surface in order to make it uniform.

B. Phosphorus Doping and Annealing

The drain region is formed by Phosphorus doping into the substrate thorough ion implantation. The implantation energy and ion dose are selected as 1KeV and 3.2×10^{18} [cm^{-3}] respectively.

After the implantation a quick activation (rapid thermal annealing) is done for 1 second at 900^0C. Finally the doping profile obtained.

C. Germanium Implantation Boron Doping and Annealing

First Germanium is doped into the source region with a pick concentration 1×10^{20} [cm^{-3}]. The Germanium concentration is confined within the source region as strictly as possible.

Then Boron is doped into the source region thorough ion implantation. The implantation energy and ion dose are

Manuscript received April 12, 2012; revised May 23, 2012.

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selected as 1KeV and 7.9×10^{19} [cm^{-3}] respectively. Then a quick thermal activation is done for 1.0 second in 900^0C.

D. Gate Insulator Formation

Next a 1nm thick Hafnium Oxide is deposited over the surface and the etched accordingly to form the gate insulator region.

E. Metal Gate Formation

After this a 1nm thick Aluminium is deposited over the surface and then etched such a way that it remains on above the gate insulator region only. The gate metal formation is done in this stage.

All the fabrication related device parameters are shown in Fig. 2, Fig. 3, Fig. 4 and Fig. 5.

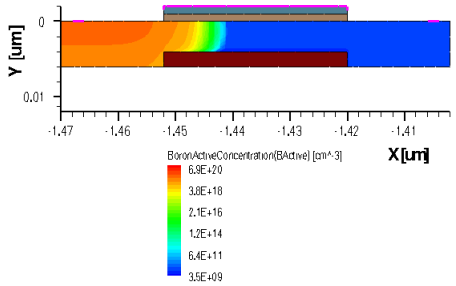

Fig. 2. Boron active concentration for fabricated device.

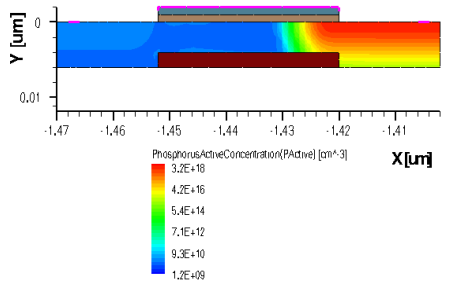

Fig. 3. Phosphorus active concentration for fabricated device.

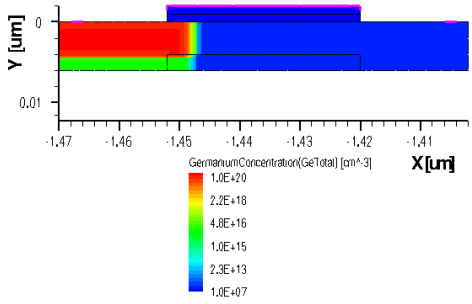

Fig. 4. Germanium concentration for fabricated device.

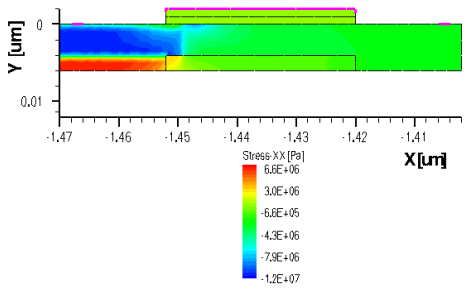

Fig. 5. Stress across XX-direction for fabricated device.

IV. Device Characteristics

In this section various device parameters are studied for this structure all the results are obtained using Sentaurus Device. The device simulations are performed using the drift-diffusion (DD) model along with the following physical models [8], [9]:

- Dynamic non-local path model for BTBT
- Masetti model for carrier mobility
- SRH model for recombination
- Fermi Dirac statistics for carrier distribution

A. Transfer and Output Characteristics

The transfer characteristics in Fig. 6, shows weak dependence on drain voltage and the drain current shows quasi-saturation at higher gate voltage which is typical of TFET. The output characteristic in Fig. 7 shows the high dependence of tunnelling current on gate voltage.

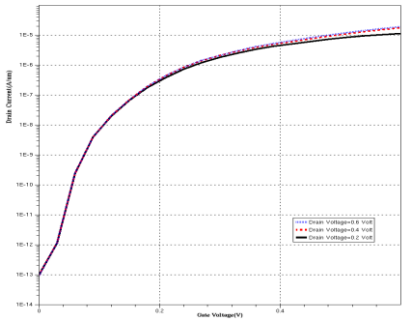

Fig. 6. Transfer characteristics at different drain voltage.

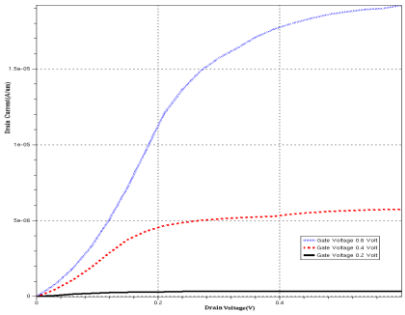

Fig. 7. Output characteristics at different gate voltage.

B. Electric Field and Band Diagram Comparison between on-State and Off-State

The comparison indicates high gate control over the band-bending at the tunnelling junction and subsequently gate control over the tunnelling current. Also the role of high Germanium mole fraction can be observed from the comparatively low band-gap at the source region. The gate increases the electric field at the tunnelling junction quite significantly as a result the tunnelling probability is also enhanced.

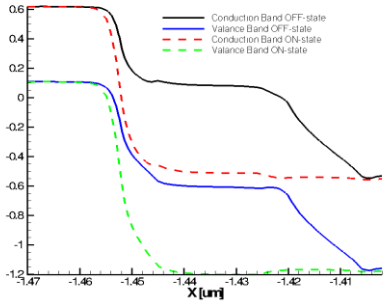

Fig. 8. Band diagram comparison at on-state and off-state.

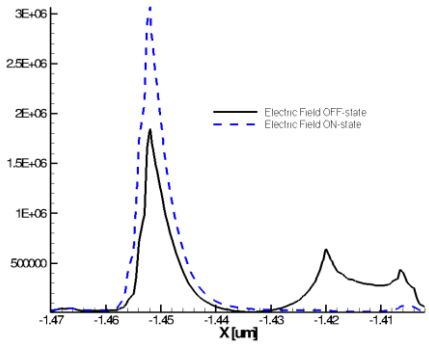

Fig. 9. Electric field comparison at on-state and off-state.

C. Physical Parameters

The values of different physical parameters are tabulated below.

Gate Length	*Supply Voltage*	*Vth*	*SS*	*Ion / Ioff*	*DIBL*
32nm	0.6	0.161	39.046	1.00×10^{8}	0.195

V. Design Parameters Study

In this section we have thoroughly studied the effect of various design parameters of the device on the Sub-threshold Swing and ON-state/ OFF-state current ratio. The initial structure is chosen as the structure shown in Fig. 1.

A. Channel Depth Study

The variation of on-state/ off-state current ratio and sub-threshold swing of the device with the substrate thickness is shown in Fig. 10.

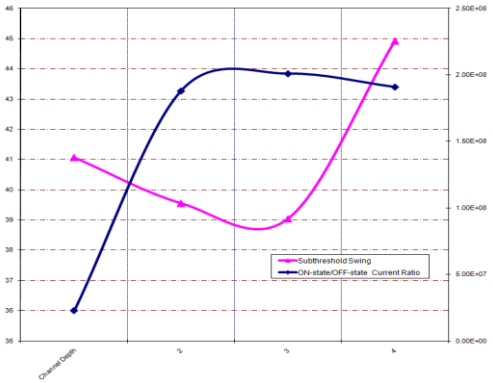

Fig. 10. Study of channel depth on Ion/ Ioff and SS.

The plot shows, sub-threshold swing first decreases then keeps increasing with increasing channel thickness and attains its minimum value at 4nm channel thickness. The on-state/ off-state current ratio keeps increasing with increasing channel thickness and then achieve quasi-saturation where it marginally decreased with increasing channel thickness. For the device structure shown in Fig. 1, the electric field at the tunneling junction decreases with increasing substrate thickness. Consequently the tunneling probability hence the tunneling current decreases. Thus for a thicker substrate in order to obtain a specific on-current, a higher gate bias is required compared to a thinner substrate. This explains the behavior of the sub-threshold curve beyond 4nm.But when the substrate is very thin, the effective density of state is very small, and therefore even if the electric field at the tunneling junction is high hence the tunneling probability is high still there are not enough states. Thus as the thickness increases gradually from a low value up to 4nm, the sub-threshold swing decreases.

B. Gate Length Study

Fig. 11 shows the variation of the on-state/ off-state current ratio and sub-threshold swing of the device with channel length.

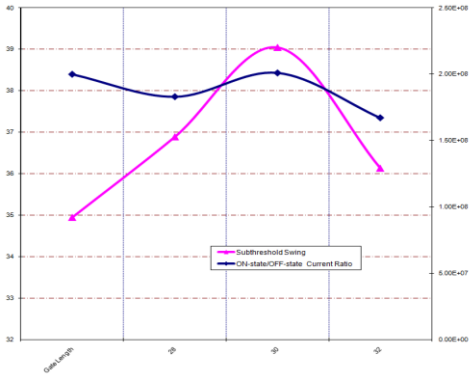

Fig. 11. Study of gate length on Ion/ Ioff and SS.

The plot shows sub-threshold swing attains its optimum value at 30nm gate length. The on-state/ off-state current ratio keeps increasing with increasing channel thickness and then decreased its optimum value achieved at 32nm gate length. The nature of variation can be explained from similar arguments given in Section 5.2.

C. Germanium Mole Fraction Study

Finally Fig. 12 shows the variation of the on-state/ off-state current ratio and sub-threshold swing of the device with Germanium mole fraction at source.

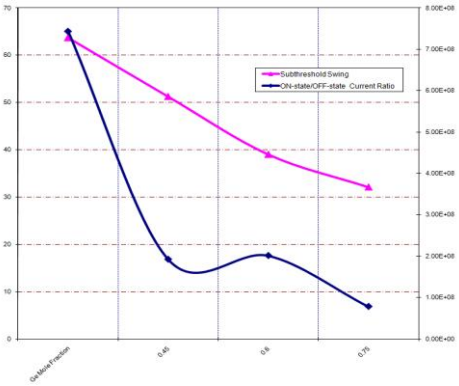

Fig. 12. Study of ge mole fraction on Ion/ Ioff and SS.

From the study it can clearly be deduced the sub-threshold swing keeps decreasing with increasing Germanium mole fraction. The on-state/ off-state current ratio also keeps decreasing then increased and again decreased with increasing Germanium mole fraction which accounts for increasing off-state current with increasing Germanium mole fraction.

VI. Conclusion

In this work we have shown a UTB SOI TFET structure which is useful for ultra-low power application. The ultra – low power application requires high on-state current and low off-state current simultaneously. At the same time extremely low sub-threshold swing is required for

aggressive supply voltage scaling. The fabricated structure meets all this criteria and shows excellent result in terms of on-state/off state current ratio and sub-threshold swing. Further the design parameters study provides an effective means to find out optimized device structure for low-power applications.

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