Reduced Master Equation as a Novel and Fast Method for Modeling of Spin Transport in Ferromagnetic Single Electron Transistors

S. Asgari and R. Faez

Abstract—**In this paper, we formulate and investigate the reduced master equation as a novel and fast simulation method of spin dependent transport in ferromagnetic single electron transistors (FMSET) which so far this method for modeling of FMSET has not been mentioned in no paper. This simulation method follows the steady state master equation in which all charge states of the system are considered, whereas the charge states decrease in reduced master equation. This method is based on two degrees of electron freedom which are charge and spin. This is applied in the condition that the orthodox tunneling theory is applicable to calculate the tunneling rate of electrons through barriers. A comparison between current-bias voltage and current-gate voltage characteristics of different ferromagnetic single electron transistors following the reduced and full master equation methods shows that the results at low bias voltages are the same. Consequently, the reduced master equation method for simulation of current-bias/gate voltage of FMSETs is more simplified and improves the speed of numerical simulation, and also the modeling results are as accurate as the results of the full master equation method at low bias conditions in current scale.**

Index Terms—**Master equation method, Single electron transistor, sequential tunneling regime, Spin.**

I. Introduction

A ferromagnetic single electron transistor (FMSET) is a novel device that offers further miniaturization of electrical device components which is a general need owing to the fact that high density memories and small and accurate sensors are essential to achieve more voluminous and faster chips[1]. A F/F/F FMSET includes a small central ferromagnetic electrode (island) coupled by tunnel barriers, to ferromagnetic source and drain leads as well as external nonmagnetic gate. The structure of such transistors is F/F/F as source/gate/drain [2]. When magnetic configuration of leads and island are parallel or anti parallel alignment, the junction resistance is low and high respectively as shown in Fig. 1. Fig. 2 is equivalent circuit of F/F/F SETs. There are three significant capacitors, first and second junctions (c_1 and c_2) and the gate capacitor (c_g), and also $c = c_1 + c_2 + c_g$ is total electrical capacitance of the island. The work done by each voltage sources to add one extra electron to the island is $E_c = e^2 / 2c$ which is called charging energy [1]-[2]-[3]-[4]-[5].

There are three different transport regimes: First sequential tunneling, which electrons tunnel consecutively one by one through barriers, second Co-tunneling that electrons flow following higher-order tunneling processes consisting tunneling of one, two or more electrons [1].The third tunneling regime is strong coupling that electrons propagate from the source to the drain and cannot localize on the island. These electrons will coherently move through the system, so perturbation theory fails [1]. If the resistances of tunnel junctions are much larger than the quantum resistance $R_1, R_2 >> R_k = \hbar / e^2 = 25.8_{k\Omega}$ strong coupling and co-tunneling (higher order processes) can be neglected but the sequential tunneling is considered. Then, first order perturbation theory gives the sequential tunneling rate. Where the discrete levels of the island are smaller than thermal energy $\Delta E < K_B T$, the distributions of the electrons on central electrode are in thermal equilibrium. Then, perturbation theory gives the sequential tunneling rate by the orthodox tunneling theory, Fermi's golden rule [1]-[3]-[15]. And also, in the sequential tunneling regime, where total electrical capacitance of the island is small enough, E_c can be significantly larger than thermal energy, $K_B T$, that leads to Coulomb blockade at low bias voltages and to characteristic 'Coulomb staircase' of electric current above a certain threshold voltage [6]-[7]-[8]-[9]-[10]-[12]-[13]-[14]. In this condition, the current in F/F/F SETs can be controlled under the influence of gate charge by the tuning gate voltage. When we keep the bias voltage for adding a charge in or removing a charge from the island, the charging energy E_c is required. When the gate voltage is tuned, two adjacent charge states become degenerate, so the electrons can be added to or removed from the island without extra energy cost and sequential tunneling current is produced [20].

Modeling of Ferromagnetic single-electron transistors is based on (I) Master Equation method, (II) the Monte Carlo method, and (III) Deterministic method. They are based high numerical intensive and need several hours to get result. However, the reduced master equation method as a novel and fast simulation method of spin dependent transport in ferromagnetic single electron transistors (F/F/F SETs) has not been mentioned in no paper, this method for modeling F/F/F SETs is more simplified and improves the speed of numerical simulation.

The essential formulations for modeling following the full

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S. Asgari is with the electrical engineering department of Sharif University of Technology, Tehran, Iran (e_asgari@alum.sharif.edu).

R. Faez is with the electrical engineering department of Sharif University of Technology, Tehran, Iran (faez@ sharif.edu).

master equation and related phenomena in F/F/F SETs are explained in Section 2. Moreover, according to the full master equation, the reduced master equation for modeling of F/F/F SETs is introduced in Section 3. In Section 4, numerical modeling results are shown and discussed. Summary and final conclusions are presented in Section 5.

II. Modeling of FMSETs Following The Steady State Master Equation

Generally, statistical mechanics and stochastic processes are required to specify the mechanism of many electrons tunneling at a junction. When an electron is added to the island, the system energy will be increased by E_c. So, the system state is defined according to the number of electrons in the island. The steady state master equation tells us about current situation of the system by calculating occupation probability of each one of discrete set of states. In the Sequential tunneling regime, the electrons tunnel consecutively one by one through barriers. This means that the state of the system with n electrons can change only to n+1electrons and n-1electrons in a neighboring state. This type of transition between different states can be understood from system states schematic in Fig. 3 [16]. It is clear that assumption of the sequential tunneling regime simplifies the analysis of stochastic process. In addition, this is important to consider that the type of electron spin is never changed during the tunneling process of electrons through potential barriers. In other words, because of the long spin relaxation time, there are no spin flip events inside the barrier region. Also, fast electronic relaxation is required to reach thermal equilibrium of electrons with a particular spin orientation. This is to say that $d_{i_\sigma,j_\sigma} >> \Gamma^L_{i_\sigma}, \Gamma^R_{i_\sigma}$ and $d_{i_\sigma,j_\sigma} >> \Gamma^L_{i_\sigma}, \Gamma^R_{i_\sigma} >> \omega_{i_\uparrow,j_\downarrow}$. $\Gamma^L_{i_\sigma}$ and $\Gamma^R_{i_\sigma}$ are the tunneling rate of electrons when electrons tunnel from the left (right) electrode to the level E_{i_σ} of the island. d_{i_σ,j_σ} is the transition probability from the level E_{i_σ} to the level E_{j_σ} ,and $\omega_{i_\uparrow,j_\downarrow}$ is the transition probability from the level E_{i_σ} to the level $E_{j_{-\sigma}}$ .Also, we suppose that the island is not small enough to consider discrete energy levels. In this condition, the island energy spectrum is discrete energy levels separated by the charging energy, $E_c = e^2/2c$. So, the island energy levels are independent of the number of electrons and the electron distributions in the central electrode, this assumption simplify the analysis of ferromagnetic single electron transistors [3]-[17]-[18]. According to the application of the master equation, mathematically, a system of ferromagnetic single electron transistor can be described by the following (1) [16].

$$\frac{\partial P_n(t)}{\partial t} = 0 = \Gamma^-_{(n+1)\sigma} P_{n+1}(\sigma) + \Gamma^+_{(n-1)\sigma} P_{n-1}(\sigma) + + (\Gamma^+_{(n)\sigma} + \Gamma^-_{(n)\sigma}) P_n(\sigma) \tag{1}$$

where $P_n(t)$ is the time dependent occupation probability of state *n*. The net tunnel rates, $\Gamma^+_{(n)\sigma}$ and $\Gamma^-_{(n)\sigma}$ are given, as in (2) and (3) [16]-[19].

$$\Gamma^+_{(n)\sigma} = \vec{\Gamma}_{L\sigma}(n) + \overleftarrow{\Gamma}_{R\sigma}(n) \tag{2}$$

$$\Gamma^-_{(n)\sigma} = \vec{\Gamma}_{R\sigma}(n) + \overleftarrow{\Gamma}_{L\sigma}(n) \tag{3}$$

In this case, $\vec{\Gamma}_{L\sigma}(n)$ ($\vec{\Gamma}_{R\sigma}(n)$) is the tunneling rate of an electron to the island through the left (right) junction. In addition, $\overleftarrow{\Gamma}_{L\sigma}(n)$ ($\overleftarrow{\Gamma}_{R\sigma}(n)$) is the tunneling rate of an electron out of the island through the left (right) junction. All the possible electron tunnel rates, $\Gamma^{\pm}_{(n)\sigma}$ for different states should be written down to prepare all of the steady state master equations.

Since the state of the system with n electrons can change only to n+1 and n-1 electrons in a neighboring state in the sequential tunneling regime, electron tunnel rates can be easily calculated from the orthodox theory in (4) [16]-[19].

$$\vec{\Gamma}_{(L/R)\sigma}(V_{ds}, V_{gs}, n) = \frac{\vec{E}_{(L/R)\sigma}(V_{ds}, V_{gs}, n)}{e^2 R_{(L/R)\sigma}[1 - \exp(-\frac{\vec{E}_{(L/R)\sigma}(V_{ds}, V_{gs}, n)}{K_B T})]} \tag{4}$$

$$\overleftarrow{\Gamma}_{(L/R)\sigma}(V_{ds}, V_{gs}, n) = \vec{\Gamma}_{(L/R)\sigma}(-V_{ds}, -V_{gs}, -n) \tag{5}$$

$\vec{E}_{(L/R)\sigma}(V_{ds}, V_{gs}, n)$ is the change in free energy of the whole circuit before and after the tunneling event through the left (right) tunnel junction. Moreover, $R_{(L/R)\sigma}$ is the resistance of the left (right) tunnel junction. $\vec{E}_{(L/R)\sigma}(V_{ds}, V_{gs}, n)$ can be described in (6) and (7)[19].

$$\vec{E}_{L\sigma}(V_{ds}, V_{gs}, n) = \frac{e}{c_1}(Q_1 - Q_{c1}) \tag{6}$$

$$\vec{E}_{R\sigma}(V_{ds}, V_{gs}, n) = \frac{e}{c2}(Q_2 - Q_{c2}) \tag{7}$$

$$Q_1 = \frac{c_1(-ne + c_2 v_{ds} + c_g v_{gs})}{c_1 + c_2 + c_g} \tag{8}$$

$$Q_2 = \frac{c_2[ne + c_1 v_{ds} + c_g(v_{ds} - v_{gs})]}{c_1 + c_2 + c_g} \tag{9}$$

$$Q_{c1} = \frac{c_1}{c_1 + c_2 + c_g}\frac{e}{2} \tag{10}$$

$$Q_{c2} = \frac{c_2}{c_1 + c_2 + c_g}\frac{e}{2} \tag{11}$$

Q_2 And Q_1 are respectively described as the charge of the left and right junctions, and also, Q_{c2} and Q_{c1} are the critical charges of the left and right junctions. All the possible charge states in the tunnel junction should be considered to solve a full master equation. In fact, at the steady state, calculating P_n is applicable by solving $\partial P_n(t)/\partial t = 0$ with the condition, $\sum P_n = 1$ which is resulted from the random process rules. Finally, at the steady state, the current through the island can be described considering that the net steady state current flowing in source junction is equal to that in drain one. Thus, the steady state current can be calculated in (12) [16]-[19].

$$I_\sigma = e\sum_{n=-\infty}^{\infty} P_n(\sigma)[\vec{\Gamma}_{L\sigma}(n) - \overleftarrow{\Gamma}_{L\sigma}(n)]$$
$$I = I_\downarrow + I_\uparrow \quad (12)$$

III. Units the Fast Modeling Method Base on the Reduced Master Equation

This method is started with considering only three charge states (n-l, n, n+l) for the system. The State transition diagram between the three charge states (n-l, n, n+l) is presented in Fig 4. Thus the steady state master equations are written down only for the three charge states (n-l, n, n+l). Then, these equations are put in matrix form similar to the full master equation. The process is shown more representatives, as in (13) [16].

$$\begin{bmatrix} -\Gamma^+_{(n-1)\sigma} & \Gamma^-_{(n)\sigma} & 0 \\ \Gamma^+_{(n-1)\sigma} & \Gamma^-_{(n)\sigma}+\Gamma^+_{(n)\sigma} & \Gamma^-_{(n+1)\sigma} \\ 0 & \Gamma^+_{(n)\sigma} & -\Gamma^-_{(n+1)\sigma} \end{bmatrix} \times \begin{bmatrix} P_{n-1}(\sigma) \\ P_n(\sigma) \\ P_{n+1}(\sigma) \end{bmatrix} = 0 \quad (13)$$

(14),(15) and (16) can be resulted from (13).

$$P_n\Gamma^-_{(n)\sigma} = P_{n-1}\Gamma^+_{(n)\sigma} \quad (14)$$

$$P_n\Gamma^-_{(n)\sigma} = P_{n+1}\Gamma^-_{(n+1)\sigma} \quad (15)$$

$$P_{n-1} = P_{n+1}\frac{\Gamma^-_{(n)\sigma}}{\Gamma^+_{(n-1)\sigma}}\frac{\Gamma^-_{(n+1)\sigma}}{\Gamma^+_{(n)\sigma}} \quad (16)$$

The condition $\sum P_n = 1$ is applied similar to the full master equation, as in

$$P_{n-1} + P_n + P_{n+1} = 1. \quad (17)$$

With substituting (14), (15) and (16) in (17), the occupation probabilities are described in (20).

$$1 = P_{n-1} + P_{n-1}\frac{\Gamma^+_{(n-1)\sigma}}{\Gamma^-_{(n)\sigma}} + P_{n+1}\frac{\Gamma^+_{(n-1)\sigma}}{\Gamma^-_{(n)\sigma}}\frac{\Gamma^+_{(n)\sigma}}{\Gamma^-_{(n+1)\sigma}} \quad (18)$$

$$P_{n-1}(\sigma) = \frac{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma}}{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^+_{(n)\sigma}} \quad (19)$$

$$\begin{bmatrix} P_{n-1}(\sigma) \\ P_n(\sigma) \\ P_{n+1}(\sigma) \end{bmatrix} = \begin{bmatrix} \dfrac{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma}}{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^+_{(n)\sigma}} \\ \dfrac{\Gamma^+_{(n-1)\sigma}\Gamma^-_{(n+1)\sigma}}{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^+_{(n)\sigma}} \\ \dfrac{\Gamma^+_{(n-1)\sigma}\Gamma^+_{(n)\sigma}}{\Gamma^-_{(n)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^-_{(n+1)\sigma} + \Gamma^+_{(n-1)\sigma}\Gamma^+_{(n)\sigma}} \end{bmatrix} \quad (20)$$

As mentioned above, the final objective calculates the current through the island. Here, the tunnel junction at the drain side is considered for applying current equation, as in (21) [3]-[16]:

$$I_\sigma = e(P_{n-1}(\sigma)[\vec{\Gamma}_{L\sigma}(n-1) - \overleftarrow{\Gamma}_{L\sigma}(n-1)] + $$
$$+ P_{n+1}(\sigma)[\vec{\Gamma}_{L\sigma}(n+1) - \overleftarrow{\Gamma}_{L\sigma}(n+1)])$$
$$I = I_\downarrow + I_\uparrow \quad (21)$$

The reduced master equation considers just the three charge states instead of all possible charge states in the full master equation. The results of the reduced and the full master equation methods are matching at low bias conditions. Moreover, the reduced master equation has the advantage of being more simplified and fast [16].

IV. Simulation Results

In order to confirm the validity of the fast introduced method, I-Vb characteristics and current-gate voltage dependences (I-Vg) with parallel and anti-parallel alignment of leads are illustrated in figures 5(a) – 9(a) by both the reduced and the full master equation methods. These are resulted with considering a FMSET with c_1= 26aF, c_2= 26aF, c_g= 9aF, E_c= 0.65meV, V_g= 50mev at a temperature of T = 0.1K .And also, junction resistances in the parallel alignment are $R_{1\uparrow}$= 400MΩ, $R_{1\downarrow}$= 100MΩ, $R_{2\uparrow}$= 8MΩ and $R_{2\downarrow}$= 2MΩ, whereas in the ant parallel configuration, the magnetization of the right electrode is reversed and then the corresponding resistances are $R_{2\uparrow}$= 2MΩ, $R_{2\downarrow}$= 8MΩ which result in Polarization , $P_j = R_{j\downarrow}/R_{j\uparrow}$, P=4. It is clear that spin asymmetry factors in the parallel configuration have been assumed the same for both left and right junctions. Owing to three small capacitors of the left and right junctions and gate, the Coulomb steps in the I-V characteristics are clearly seen, the length of steps are approximately equal to V_c=$(2E_c/e)(c/c_1)$~6mv which correspond to opening a tunneling channel with a new value of the excess electron with up or down spin on the island. Note, since three charge states are just considered in this method, there is not more than three steps when the reduced master equation has been used for modeling the transistors. The position of the steps is seen in the d(I parallel)/dVb and d(I parallel)/dVb curves which shown in Fig.10 and Fig.11, clearly.

Then, the comparison is made with 8 different main parameters of the F/F/F SET in figures 5– 9. These 8 different main parameters are gate capacitances, c_g, gate voltage bias, V_g, temperatures, T tunneling resistances R, and at last, polarization, P. And also, the star and square curves represent respectively the current for parallel and antiparallel configurations by the reduced master equation method and the solid and point curves represent respectively the current for parallel and ant parallel configurations by the full master equation method. The result with ifferent tunneling resistances R is shown in Fig. 5(b) that the junction resistances in the parallel alignment are: $R_{1\uparrow}$= 200MΩ, $R_{1\downarrow}$= 50MΩ, $R_{2\uparrow}$= 2MΩ and $R_{2\downarrow}$= 8MΩ, whereas in the ant parallel alignment $R_{2\uparrow}$= 8MΩ, $R_{2\downarrow}$= 2MΩ. In Fig 6.b Vg is changed to 27mV, then in Fig 7.b T = 1.5K and in Fig 8.b C_g = 19aF. At last, in Fig 9.b P=1.8. The results of these comparisons show that the simulation results by both; the reduced and the full master equation methods; are the same for all main parameters at low bias voltages $eV_b < 3E_c$ which supply in current scale.

In addition to confirm this modeling method, the I-Vg characteristics by the reduced and the full master equation are respectively represented by the solid and point curves. Three constant bias voltages which are above the threshold voltage have been assumed from eVb = $0.25E_C$(bottom) to $0.75E_C$ (top) in Fig. 10. Where the bias voltage is kept below the Coulomb voltage and the gate voltage increased the energy of

the system with one extra electron decreases and the energy of the initial system increases and two adjacent charge states become degenerate. Then, the Coulomb blockade is broken and the electrons can enter or leave the island and produce the sequential tunneling current. Ideally, the lowest and highest amount of current are respectively $V_g = 0$ and $e/2C_g$, and also it can be periodically modulated with a period of $V_g = e/C_g$ like current-gate voltage dependences (I-Vg) in Fig. 10.The solid and point curves under $eV_g=3E_c$ (three charge states) are the same and the discrepancy between them above of that gate voltage is quite obvious. Consequently, the reduced master equation method for simulation of current-bias/gate voltage of F/F/F SETs is more simplified than the full one and improves the speed of numerical simulation. Also, since the discrepancy between both methods is insignificant and can be neglected in current scale, the full master equation method can be approximated by the reduced one at low bias conditions.

Moreover, the I-Vb and I-Vg characteristics of a FMSET by the reduced and the full master equation methods are not exactly the same and there is an insignificant discrepancy between the results which is obvious in Fig.10 and Fig.11. These are the d(Iparallel)/dVb and d(Iparallel)/dVb curves by both methods which can proof that the difference between the results of full and reduced master equation methods can be neglected.

However, Tunneling Magnetoresistance $\mathbf{TMR\%} = 100\,(I_p - I_{AP})/I_p$ is the property of F/F/F SETs (magnetic tunnel junctions) to change the value of its electrical resistance when an external magnetic field is applied to its ferromagnetic leads changed. TMR is one of very important parameter of FMSETs and is so sensitive to the exact amount of current, so the difference between current results by two methods can be extremely clarified when Tunneling Magnetoresistance is studied. The Tunneling Magnetoresistance of a F/F/F SET by both the Full and the reduced master equation methods are respectively illustrated in Fig. 11 and 12. According to Fig. 11, TMR oscillates with increasing bias voltage with the period of the current steps length $V_c = (2E_c/e)(c/c_1)$~6mv and also, the amplitude of the oscillations diminishes with increasing bias voltage. In Fig. 12, TMR is not similar to Fig. 11 and quite disturbed because of the discrepancy between current results by two methods. This discrepancy cannot be neglected to calculate TMR. So the reduced master equation is not valid to calculate TMR since insignificant discrepancy between F/F/F SET currents by two methods in current scale is appeared in the calculated TMR.

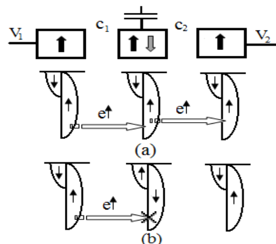

Fig. 1. (a): Parallel state, the majority electrons in the left electrode tunnel into the majority band of the right electrode. Junction resistance of the parallel configuration is low. (b): Antiparallel state, the minority electrons in the left electrode tunnel into the majority band on the opposite side of the barrier. Junction resistance of the antiparallel configuration is high.

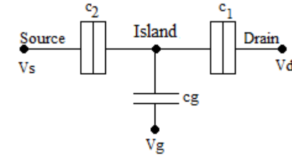

Fig. 2. The equivalent circuit of a single-electron transistor.

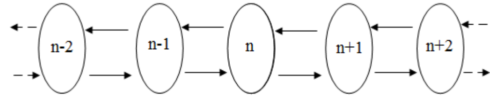

Fig. 3. State transition diagram for SET device.

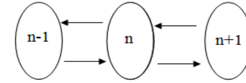

Fig. 4. State transition diagram for SET device considering only three charge states.

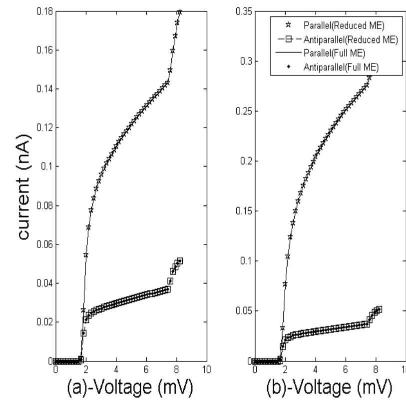

Fig. 5. The I-V characteristics of a ferromagnetic single-electron transistor for (a): R1↑= 400MΩ, R1↓= 100MΩ, R2↑= 2 MΩ and R2↓= 8MΩ, whereas in the antiparallel alignment R2↑= 8 MΩ, R2↓= 2 MΩ and (b): R1↑= 200MΩ, R1↓= 50MΩ, R2↑= 2 MΩ and R2↓= 8 MΩ.

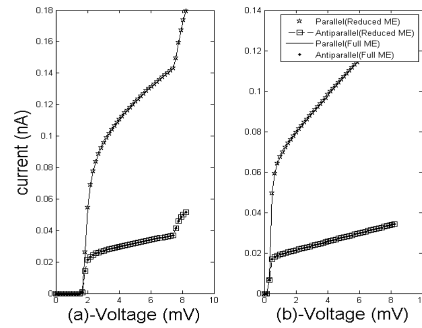

Fig. 6. The I-V characteristics of a ferromagnetic single-electron transistor for (a): Vg = 50 meV, and (b): Vg = 27 meV.

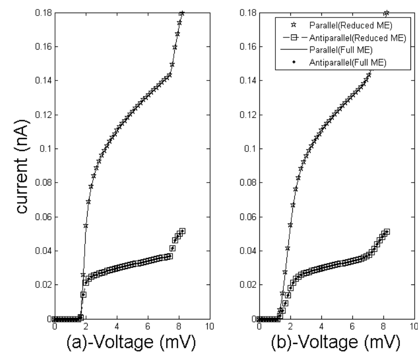

Fig. 7. The I-V characteristics of a ferromagnetic single-electron transistor for (a): T = 0.1 K, and (b): T = 1.5 K.

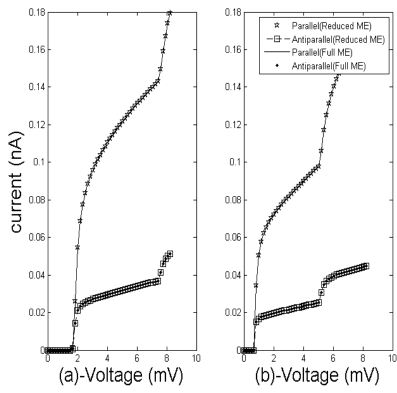

Fig. 8. The I-V characteristics of a ferromagnetic single-electron transistor for (a): cg = 9aF, and (b): cg = 19aF.

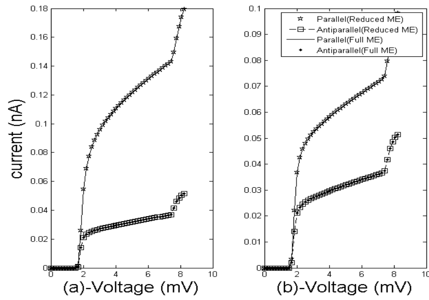

Fig. 9. The I-V characteristics of a ferromagnetic single-electron transistor for (a): P=4, and (b): R1↑ = 360MΩ, R1↓ = 200MΩ, R2↑ = 4 MΩ and R2↓ = 7.2 MΩ, whereas in the antiparallel alignment R2↑ = 7.2MΩ, R2↓= 4MΩ which means P=1.8.

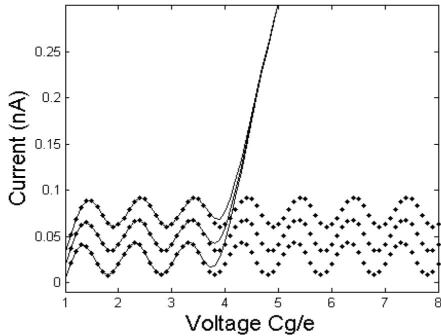

Fig. 10. The I-Vg characteristics by the reduced and the full master equations are respectively represented by the solid and point curves from eVb = 0.25EC(bottom) to 0.75EC (top).

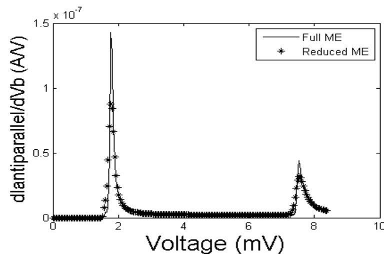

Fig. 11. The d(Iparallel)/dVb curves by both the reduced and the full master equation methods

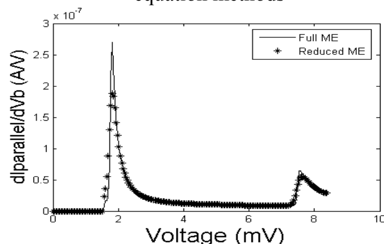

Fig. 12. The d(Iparallel)/dVb curves by both the reduced and the full master equation methods

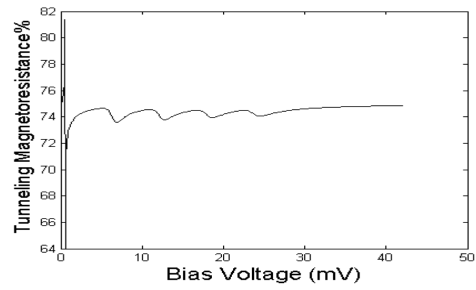

Fig. 13. TMR oscillates with increasing bias voltage with the period the $V_c=(2E_c/e)(c/c_1)$~6 following the full master equation method.

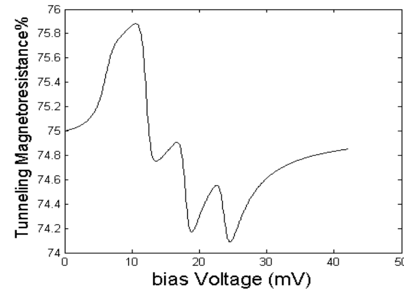

Fig. 14. TMR following the reduced master equation method.

V. CONCLUSION

Briefly, in this paper we formulated a new simulation method of spin dependent transport in the F/F/F SET. This simulation method follows the steady state master equation in which all charge states of the system are considered, whereas the charge states decrease in the reduced master equation. This method is based on two degrees of electron freedom which are charge and spin. This is applied in the condition that the orthodox tunneling theory is applicable to calculate the tunneling rate of electrons through barriers. The comparison between IV_b and IV_g characteristics of F/F/F SET following the fast and the full master equation methods for different gate capacitance, c_g, junction resistances R, gate voltage bias, V_g, polarization, P, temperatures, T, and at last different bias voltage is made and shows that the simulation results are exactly the same at low bias voltages in current scale. And also, the reduced master equation is not valid to calculate TMR since insignificant discrepancy between F/F/F SET currents by two methods in current scale is appeared in the calculated TMR. So, the reduced master equation method is not only more simplified and improves the speed of numerical simulation, but also with the exception of discrepancy in scales of 10^{-20} its current results are nearly the same as the results of the full maser equation method at low bias conditions.

REFERENCES

[1] J. Barnas and I. Weymann "Spin effects in single electron tunneling" J. Phy.: Condens. Matter 20, 423202, 2008.

[2] M. Urech, Spin-dependant transport in lateral nano-devices based on magnetic tunnel junctions. PhD thesis, Stockholm, Sweden, 2006.

[3] J. Barnas, J. Martinek, G. Michalek, B. R. Bulka, and A. Fert" Spin effects in ferromagnetic single-electron transistors", Phys. Rev. B Vol.62,PP.12363, 2000.

[4] J. Wiśniewska and I. Weymann"Theoretical analysis of transport in ferromagnetic single-electron transistors in the sequential tunneling regime" Mat. Science (Poland) Vol.26, No. 3, PP.715, 2008.

[5] R P. Andres, T Bein, M Dorogi, S Feng, J I. Henderson, C P. Kubiak, W Mahoney, R G. Osifchin, R. Reifenberger," Coulomb Staircase at

Room Temperature in a Self-Assembled Molecular Nanostructure," Science, Vol. 272, no. 5266, pp. 1323 – 1325, 1996.
[6] A. E. Hanna and M. Tinkham" Variation of the Coulomb staircase in a two-junction system by fractional electron charge" Phys. Rev. B, Vol. 44, PP. 5919–5922, 1991.
[7] T. Sato and H. Ahmed "Observation of a Coulomb staircase in electron transport through a molecularly linked chain of gold colloidal particles," Appl. Phys. Lett. Vol.70, PP. 2759, 1997.
[8] H. Imamura ,J. Chiba, S. Mitani, K. Takanashi, S. Takahashi, S. Maekawa, and H. Fujimori "Coulomb staircase in STM current through granular films" Phys. Rev. B, Vol.61, PP.46–49, 2000.
[9] J. G. A. Dubois, J. W. Gerritsen, S. E. Shafranjuk, E. J. G. Boon, G. Schmid and H. van Kempen" Coulomb staircases and quantum size effects in tunnelling spectroscopy on ligand-stabilized metal clusters" Europhys. Lett.Vol.33, PP. 279, 1996.
[10] P. Radojkovic, M. Schwartzkopff, M. Enachescu, E. Stefanov, E. Hartmann, and F. Koch" Observation of Coulomb staircase and negative differential resistance at room temperature by scanning tunneling microscopy" J. Vac. Sci. Technol. B, Vol.14, PP.1229,1996.
[11] P. John Thomas, G. U. Kulkarni and C. N. R. Rao" Effect of size on the Coulomb staircase phenomenon in metal nanocrystals ," Chemical Physics Letters, Vol.321, Issues 1-2, PP.163-168, 2000.
[12] A. I. Yakimov, V. A. Markov, A. V. Dwrechenskii, O. P. Pchelyakov "Coulomb staircase in a Si/Ge structure" Philosophical Magazine Part B, Vol.65, Issue 4, PP.701 – 705, 1992.
[13] M. Field, C. G. Smith, M. Pepper, D. A. Ritchie, J. E. F. Frost, G. A. C. Jones, and D. G. Hasko "Measurements of Coulomb blockade with a noninvasive voltage probe," Phys. Rev. Lett, Vol.70,PP.1311–1314,1993.
[14] C. W. J. Beenakker "Theory of Coulomb-blockade oscillations in the conductance of a quantum dot," Phys. Rev. B 44, 1646–1656, 1991.
[15] J. Martinek, J. Barna, G. Micha ek, B. R. Bu ka and A. Fert" Spin effects in single-electron tunneling in magnetic junctions "Journal of Magnetism and Magnetic Materials .Vol.207, Issues 1-3, PP.1-6, 1999.
[16] M.Y.A.Ismail, R.A.AbdelRassoul, "A New Fast and Accurate Steady State Master Equation Model for Capacitively- Coupled Single-Electron Transistor (SET)," IEEE, Vol.0, PP.1 – 10, 2006.
[17] K. Pappert,"Fabrication and Test of Ferromagnetic Single-Electron-Transistors," PhD thesis, Royal Institute of Technology, 2004.
[18] M. Urech, "Spin-dependant transport in lateral nano-devices based on magnetic tunnel junctions," PhD thesis, Stockholm, Sweden, 2006.
[19] P N Hai, S Sugahara, and M Tanaka "Reconfigurable Logic Gates Using Single-Electron Spin Transistors" Jpn. J. Appl. Phys, Vol.46, PP. 6579-6585, 2007.

S. Asgari, was born in Iran- Tehran in 1984 and has been graduated from Sharif University of Technology, the best university in Iran, since 2009 in electrical engineering (Master of Science)

She is working as a Supervisor of Industrial Electronics laboratory and Microprocessors and computers in Damavand branch of Islamic Azad University and was Supervisor of Computer components laboratory and a Research Assistant in department of electrical and computer engineering in Garmsar branch. Moreover, she was working as a Research Assistant in department of electrical engineering in Sharif University of Technology. Her research interest are Nanoelectronics and nanoscale devices such as few-electron devices, hybrid SET, single electron memory, nanowires, double quantum dot, double quantum well and thin films, nanostructures, Magnetism, spin transport, spintronics, magnetic devices, ferroelectric field effect MOS transistor and magnetic.

Ms. Asgari is selected and awarded as the best student, ranked 1st, with the highest GPA among all electrical engineering B.Sc. students of EE department in 2007.and selected as the best lecturer in 13th Iranian Student Conference on Electrical Engineering (ISCEE 2010).